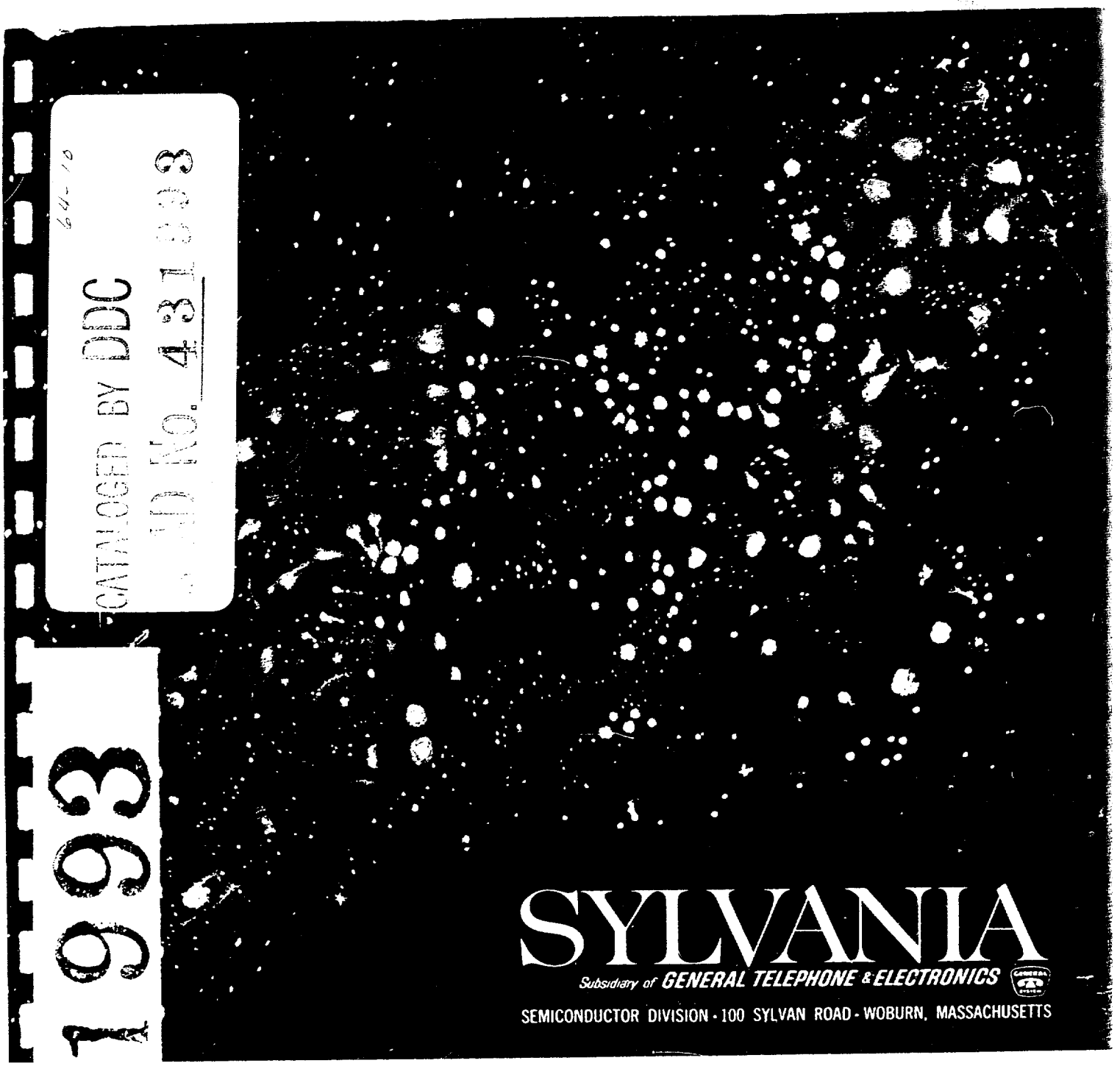

NAVY DEPARTMENT BUREAU OF SHIPS ELECTRONICS DIVISION

"DEVELOPMENT OF EPITAXIAL TECHNOLOGY FOR MICROELECTRONICS AND LARGE AREA DEVICE APPLICATION"

Quarterly Report No. 7
1 November 1963 - 31 January 1964

Contract NObsr 87431
Index Number SR-0080302, ST-9348

UNCLASSIFIED

SEVENTH QUARTERLY REPORT

FOR

"DEVELOPMENT OF EPITAXIAL TECHNOLOGY FOR MICROELECTRONICS AND LARGE AREA DEVICE APPLICATION"

This report covers the period 1 November 1963 thru 31 January 1964

SYLVANIA ELECTRIC PRODUCTS INC.
Semiconductor Division
Woburn, Massachusetts

NAVY DEPARTMENT BUREAU OF SHIPS ELECTRONICS DIVISION

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PURPOSE

The purpose of this project is the continued investigation and improvement of silicon epitaxial technology in order to make its advantages available for use in microelectronic circuits; large area, high voltage junction devices, and four layer PNPN devices.

ABSTRACT

The study of epitaxial layer thickness and resistivity for integrated circuit N/P material was completed. Work on epitaxial layer perfection was continued and the importance of the substrate perfection and surface cleaning established. The feasibility of three point probe and junction capacitance techniques on a step-etched sample for the determination of layer doping profile was investigated. Experiments on "in situ" CO_2 - $SiCl_4$ oxide growth immediately after epitaxial deposition were started. Epitaxial deposition on peripheral oxide-masked substrates was investigated. The Sylvania double-bevel technique was successfully used to determine doping profiles in N+ prediffused N/P planar circuit structures. Work on vapor phase deposition of thin silicon films on non-silicon dielectric substrates was continued.

DETAILED TECHNICAL REPORT

1.0 Epitaxial Growth of Silicon Film Over Single Crystal Silicon Substrates

1.1 Control of Layer Thickness and Resistivity in Epitaxial Wafers for Integrated Circuit Applications

The N/P epitaxial wafers used for the fabrication of integrated circuits have been grown in the standard Sylvania vertical RF furnaces. The procedure has been standardized and a high degree of control of layer thickness and resistivity has been obtained. The sum up, careful control of gas flow pattern and system geometry, plus uniform substrate temperature, allows one to control layer thickness. Carefully controlled gas phase composition in the deposition furnace, plus the judicious choice of a doping system, allows one to achieve layer resistivity control. Of course, a clean system and an ultra pure gas ambient are necessary. System contamination has been kept to a minimum by using an all-silicon and water-cooled quartz epitaxial furnace. Only silicon parts are heated during epitaxial deposition.

As reported previously, hydrogen used for the system is of very high purity. It is usually obtained by means of either a palladium diffusion unit or liquid nitrogen cooled charcoal trap, followed by an ultrafilter. These provisions account for the degree of success in obtaining good control in layer thickness and resistivity for all types of epitaxial layer structures, including those for integrated circuit applications.

The layer resistivity and thickness readings of integrated circuit epitaxial growth runs in July, 1963, and Jan., 1964, are listed in TABLE I. The layer resistivity was determined by four point probe, using a Fells probe head and an L&N K-3 potentiometer.

In FIGURE 1, the relative resistivity is plotted with the mid-point of the specified resistivity range as the reference. The two horizontal lines above and below give the limits of the resistivity specification. It is seen that there have been no runs

TABLE I

RELATIVE LAYER RESISTIVITY AND THICKNESS OF EPITAXIAL N/P WAFERS FOR SILICON INTEGRATED CIRCUITS

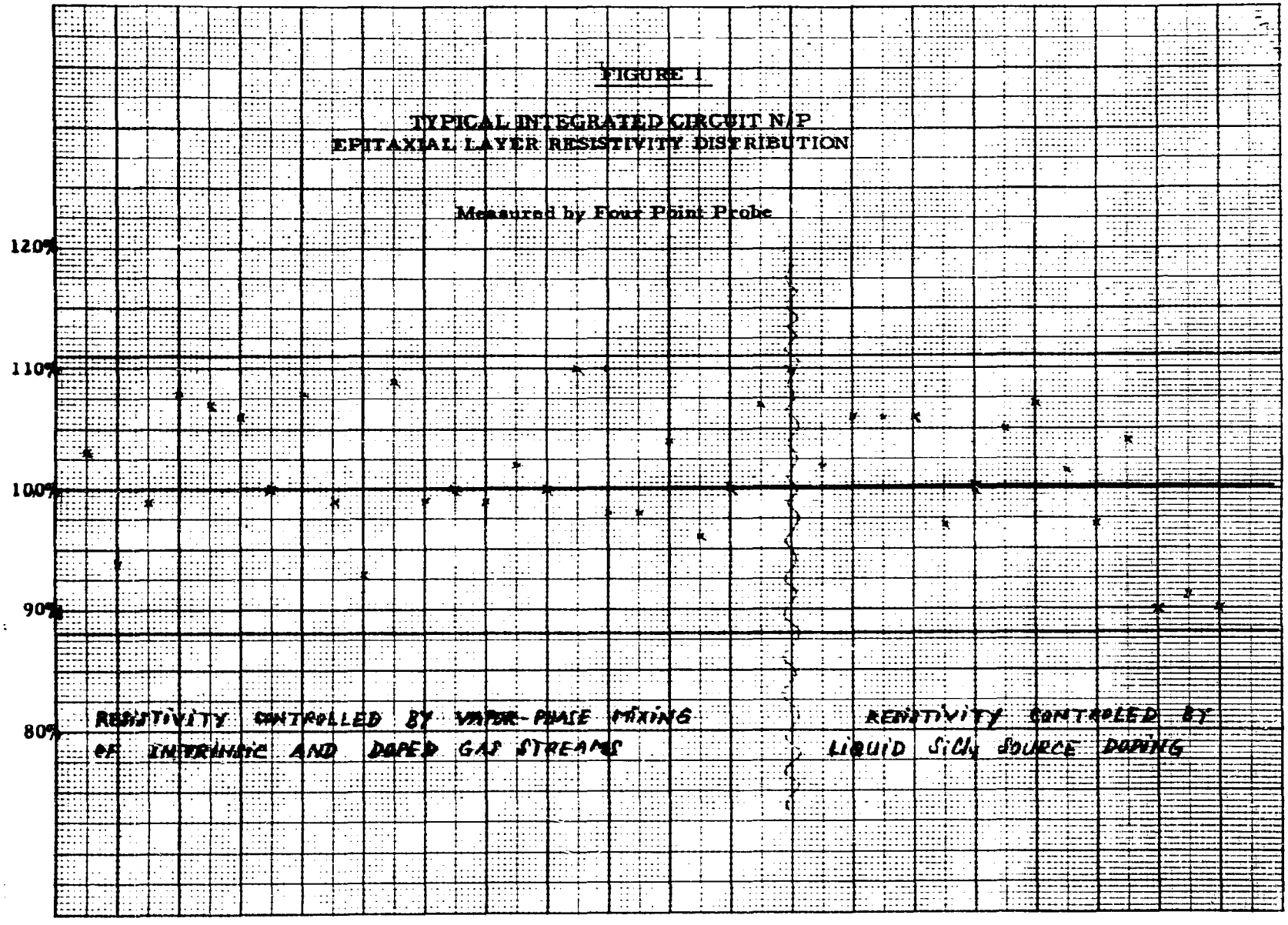
	Relative Layer Resistivity	Relative Layer Thickness		
		Trailing edge	Center	Leading edge
Run No.	% mid-point resistivity specification	% center reading of first run		
MG-548	90	95	100	98
MG-550	103	90	90	90
MG-551	94	95	98	98
MG-552	99	95	95	95
MG-553	108	95	103	98
MG-554	107	90	90	95
MH-1	106	90	90	95
MH-2	100	90	90	95
MH-3	108	85	90	95
MH-4	99	95	95	95
MH-5	93	90	95	95
MH-6	109	85	90	95
MH-7	99	98	98	98
MH-8	100	90	90	90
MH-9	99	95	98	98
MH-10	102	85	85	85
MH-11	100	95	97	95
MH-13	110	90	90	95
MH-14	98	85	85	85
MH-15	98	95	98	98
MH-16	104	95	95	95
MH-17	96	85	95	95
MH-18	100	95	106	98
MH-19	107	85	95	90
MG-200	110	-	-	- *
MG-207	102	90	98	95
MG-208	106	90	90	90
MG-209	106	90	90	90
MG-210	106	95	95	95
MG-216	97	95	95	95
MG-217	100	95	98	98
MG-218	105	95	95	95
MG-219	107	-	-	- *
MG-229	101	-	-	- *
MG-230	97	85	85	90
MG-235	104	95	95	95
MG-238	90	-	-	- *
MG-239	91	95	98	98
MG-240	90	90	95	90

*a different thickness was specified for these growth runs.

FIGURE 1

TYPICAL INTEGRATED CIRCUIT N/P
EPITAXIAL LAYER RESISTIVITY DISTRIBUTION

Measured by Four Point Probe



JANUARY 1964 RUNS

JULY 1963 RUNS

with resistivity readings out of specification. The run to run variation for all growth runs is within ± 10 per cent, which is also the accuracy of the four point probe measurement.

The layer thickness readings are obtained by a bevel-staining technique reported previously. Three sets of readings are listed: leading edge, center and trailing edge of the wafer, according to the gas flow pattern in the furnace. In FIGURE 2, the layer thickness at the center of the first run is arbitrarily chosen as the reference, or unity, and the distribution of thicknesses relative to this is plotted. If the readings in each run coincide with each other, they are represented by only one point. It is seen that the layer thickness uniformity is under good control. Variation in layer thickness in the same run is less than ± 5 per cent. From one run to the next, layer thickness uniformity within ± 5 per cent is typical with a maximum variation ± 10 per cent.

It is believed that the accuracy of present techniques used for layer thickness and resistivity measurements is comparable to the degree of control achieved. It is believed that this is the limit of our present epitaxial furnace design for these particular epitaxial wafer structures. This task is now completed.

1.2 Study and Improvement of Epitaxial Layer and Surface Perfection

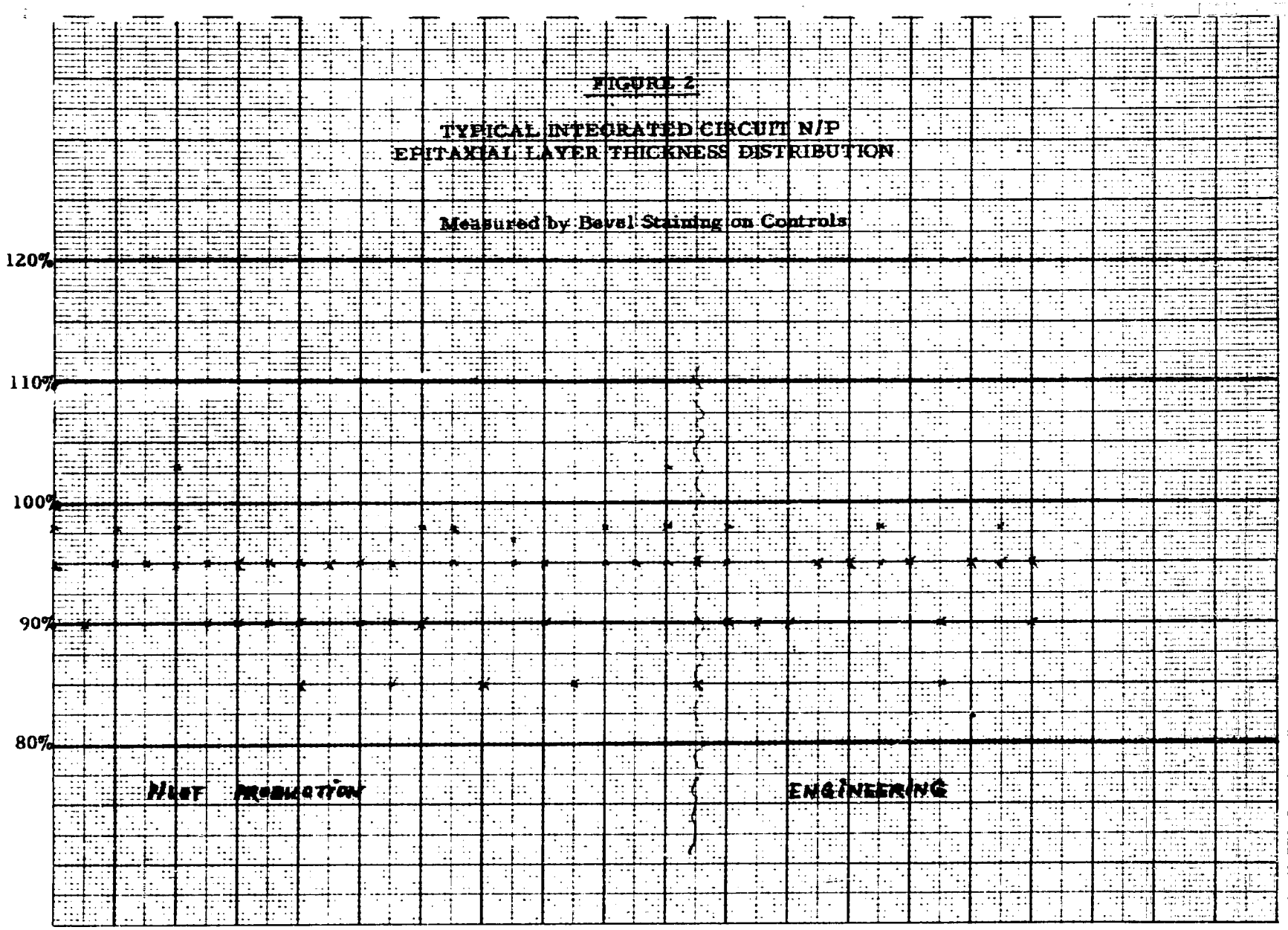
As reported previously, the epitaxial layer and surface perfection is determined by three major factors: the substrate, structural, and surface perfection; the substrate surface cleaning; and the epitaxial deposition conditions. In order to achieve epitaxial layer perfection in N/P integrated circuit epitaxial wafers, the P-type silicon single crystals have been examined and selected by X-ray diffraction techniques; particularly by the extinction contrast method.[1] Dislocations and other crystallographic defects in the crystals are also examined by an etching technique using the tentative ASTM process. The X-ray diffraction micrograph

(1) G. H. Schwuttke, Sylvania Technologist Vol. XIII, p. 122 (1960)

FIGURE 2

TYPICAL INTEGRATED CIRCUIT N/P
EPITAXIAL LAYER THICKNESS DISTRIBUTION

Measured by Bevel Staining on Controls



of a typical high quality P-type substrate slice is shown in FIGURE 3, where the dislocation density is much less than $100/cm^2$. The substrate surface preparation is generally by chemical polishing. Electrochemical polishing has also been used occasionally where smooth and uniform surfaces are needed but the process is more involved and, therefore, less frequently used.

An infrared transmission technique has also been used to examine the structural perfection of the substrates as reported in the Sixth Quarterly Report. It detects cracks, chipped edges, other types of mechanical damages, and dirt or foreign particles on the slice surface. FIGURE 4 shows a slice with a chipped edge and its associated crack, and FIGURE 5 shows wax particles on the surface of the slice. Examination of these slices by the infrared birefingance technique reveals no strain, probably due to the limitation of sensitivity of this process.

The standard substrate cleaning procedure was discussed in detail in the Fifth Quarterly Report. With careful chemical cleaning and furnace loading in a clean environment, layer stacking fault density of less than $200/cm^2$ was consistently obtained. Some work on vapor etching of the silicon substrate immediately prior to epitaxial deposition was reported in the Fifth Quarterly Report. When hydrogen chloride is used for vapor phase etching and palladium-diffusion purified hydrogen is used throughout the deposition cycle, further improvement in layer structural perfection is achieved. The layers show practically no stacking faults whatsoever, except on the very edges of the wafers. A typical layer grown with no "in situ" HCl etching is shown in FIGURE 6, and a typical layer grown with wet cleaning HCl vapor etching, and hydrogen bake is shown in FIGURE 7. The HCl "in situ" etching is a recommended practice. Extreme caution must be taken, however, to assure the purity of the HCl gas.

The task on substrate cleaning procedure is completed.

FIGURE 3

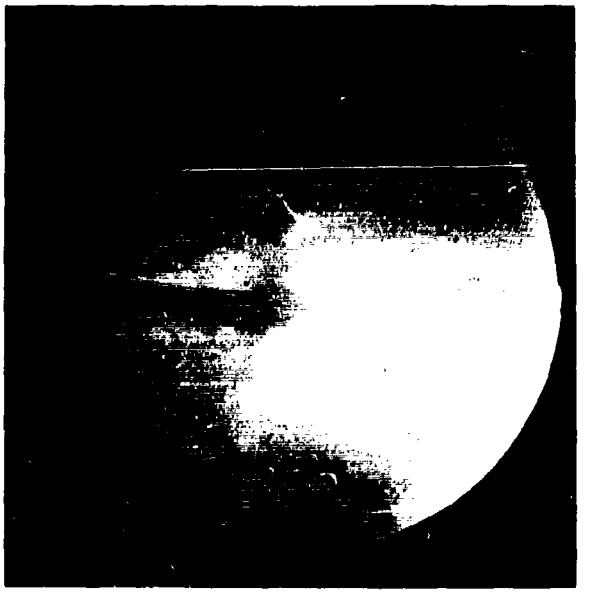
X-RAY EXTINCTION PHOTOMICROGRAPH OF 10 ohm-cm P-TYPE SILICON SUBSTRATE FOR INTEGRATED CIRCUIT EPITAXIAL LAYERS

(Chemically polished surface)

Slice Diameter
~ 1 inch

FIGURE 4

CHIPPED EDGE AND ITS ASSOCIATED CRACK IN A SILICON SUBSTRATE SLICE REVEALED BY INFRARED TRANSMISSION INSPECTION



MAGNIFIED
150 TIMES

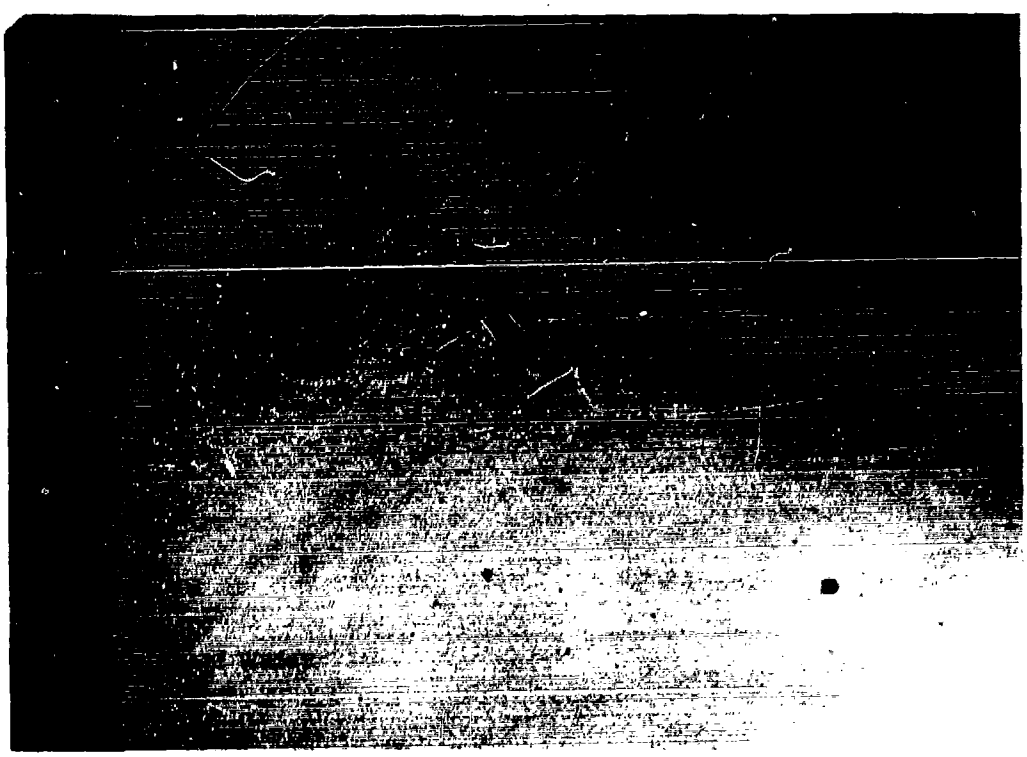
FIGURE 5

WAX PARTICLES ON A SILICON SUBSTRATE SLICE
SURFACE REVEALED BY INFRARED INSPECTION

MAGNIFIED
150 TIMES

FIGURE 6

LAYER STRUCTURAL PERFECTION OF TYPICAL EPITAXIAL WAFER WITHOUT HCl ETCHING



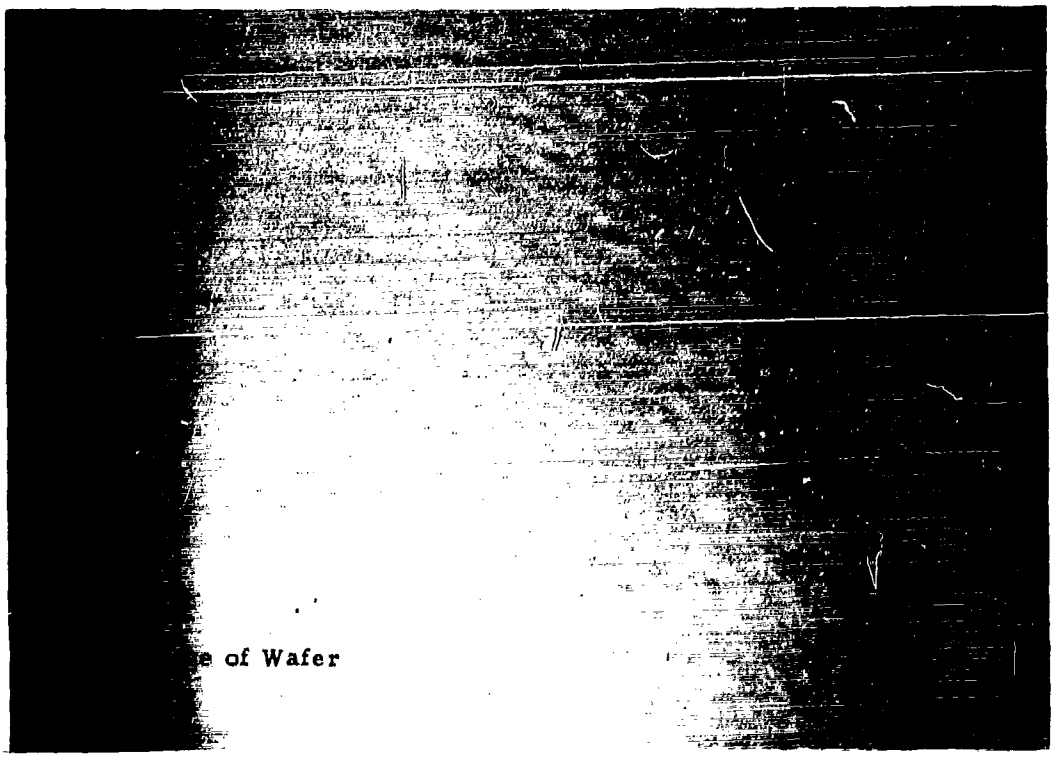
MAGNIFIED
80 TIMES

Electropolished Substrate

Chemically Cleaned Prior to Deposition

FIGURE 7

LAYER STRUCTURAL PERFECTION OF A TYPICAL EPITAXIAL WAFER WITH HCl ETCHING



MAGNIFIED
80 TIMES

Electropolished Substrate

Chemically Cleaned and HCl-Etched Prior to Deposition

1.3 Three Point Probe Process for Layer Resistivity Determination

The correlation of the P-type silicon layer resistivity and the three point probe breakdown voltage measurements was performed. The resistivity range covered by the measured samples was 0.3 to 8 ohm-cm. The results are shown in FIGURE 8.

In order to obtain similar breakdown characteristic curves for all the samples, a surface treatment was necessary. A few seconds' soak in hydrofluoric acid was found to be sufficient to make the breakdown curves similar and reproducible.

Further, it was also found that the measurements had to be made at a higher current level than was required for the N-type silicon material. The current level which had to be used to obtain readings on the P-type samples was too high for the present D.C. or the pulse technique equipment. The measurements were therefore done only with the A.C. three point probe.

1.4 Capacitance Measurements of Boron Doping Gradient Profile in P-Type Layers

When capacitance measurement is used to determine the doping profile, the region of measurement is limited to the depletion layer width at the breakdown voltage. Therefore, if a doping profile is to cover a fairly large distance, more than one P-N junction diode must be used, and the junction position must be varied along the profile. The portions of the profile can then be determined from the individual diodes, and the entire profile can be put together from the set of measurements.

The previously reported P/P+ profile measurements were accomplished by using tapered epitaxial layers. Since the layer was tapered, the distance from the P-N junction to the epitaxial substrate varied across the slice. For more recent measurements the variation of junction position has been accomplished by selective etching of a very thin portion of the epitaxial layer. By masking and etching, steps have been etched across the slice. Approximately 8 steps (about 2 microns high)

AC THREE POINT PROBE CALIBRATION FOR P TYPE SILICON

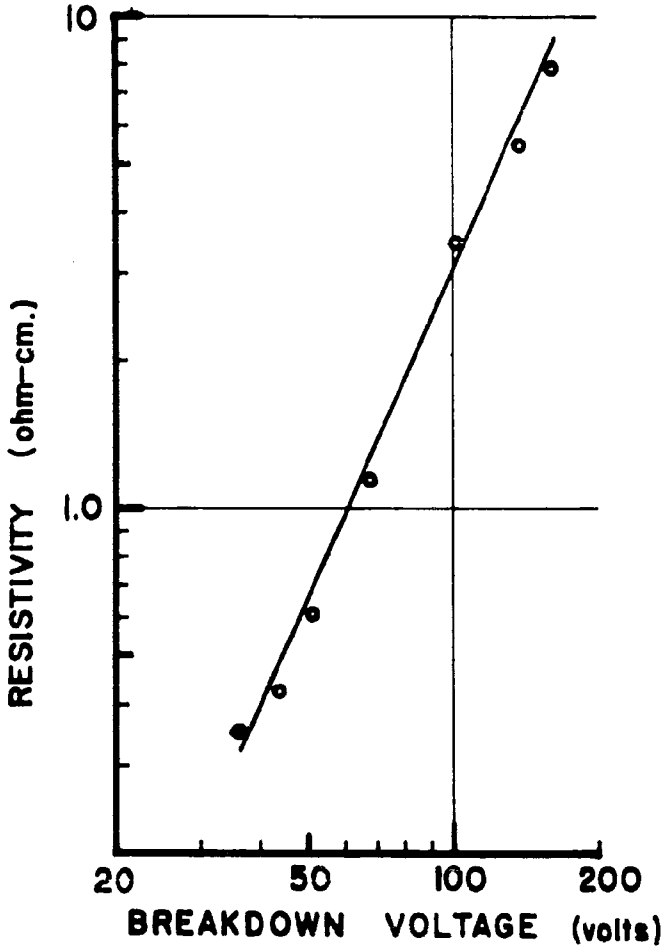


FIGURE 8

are etched before the diodes are fabricated by diffusion.

Layers up to 20 microns thick have been used, and the P/P+ profile can be determined completely by this method. The measurements can be made through the entire layer and into the heavily doped substrate. Two of these profiles are shown in FIGURES 9 and 10.

Three point probe breakdown is also measured on each step of the slice before diffusion of the diodes. An approximate profile can be determined from these measurements as shown in FIGURE 11.

This task has been completed.

1.5 "In Situ" Oxidation of Epitaxial Silicon Surface

In an attempt to improve the technology of obtaining large area, high voltage diffused epitaxial diodes, use of oxidation techniques for "in situ" slice oxidation immediately after epitaxial growth have been investigated. The idea of "in situ" oxidation assumes that the freshly grown epitaxial layer may give superior diode characteristics if the oxide used for passivation of the silicon surface is grown immediately after the growth of the epitaxial layer, and epitaxial layer is not exposed to the air ambient.

The process involves the addition of small percentages of purified CO_2 gas to the main H_2 gas stream in the epitaxial furnace, while the slices are at elevated temperatures. Two alternatives have been investigated - one in which intrinsic $SiCl_4$ is added to the gas stream (to supply the Si for the formation of SiO_2), and the other in which the silicon slices themselves supply the Si for the formation of SiO_2. The former method results in a much faster growth rate of SiO_2. Typically, a 6000 Å oxide layer can be grown in five minutes at a temperature of about 1300°C with 2% CO_2.

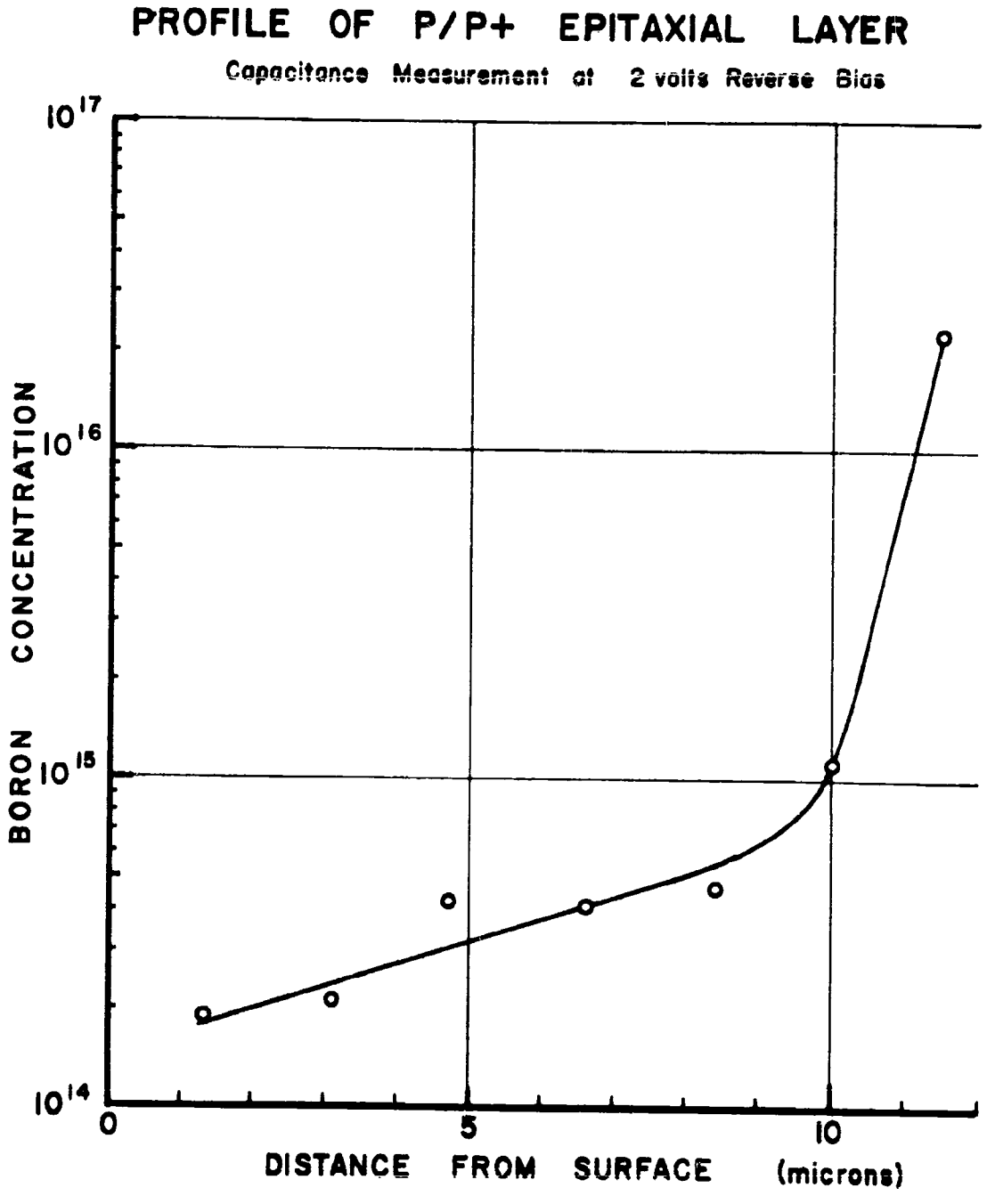

PROFILE OF P/P+ EPITAXIAL LAYER
Capacitance Measurement at 2 volts Reverse Bias
BORON CONCENTRATION
10^{17}
10^{16}
10^{15}
10^{14}
0
5
10
DISTANCE FROM SURFACE (microns)

FIGURE 9

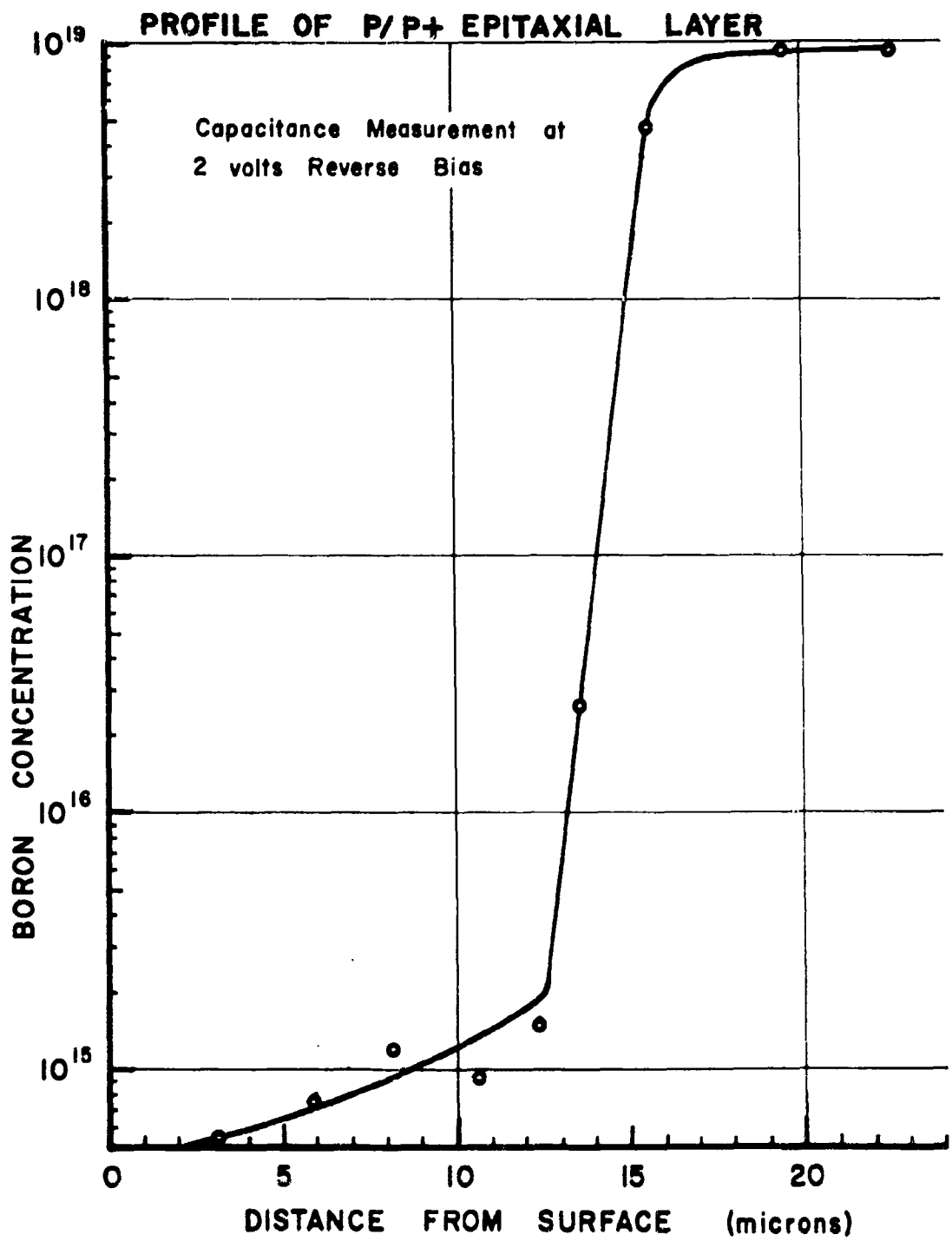

PROFILE OF P/P+ EPITAXIAL LAYER
Capacitance Measurement at
2 volts Reverse Bias
10^{19}
10^{18}
10^{17}
10^{16}
10^{15}
BORON CONCENTRATION
0
5
10
15
20
DISTANCE FROM SURFACE (microns)

Figure 10

PROFILE OF P/P+ EPITAXIAL LAYER

Measured by Three Point Probe

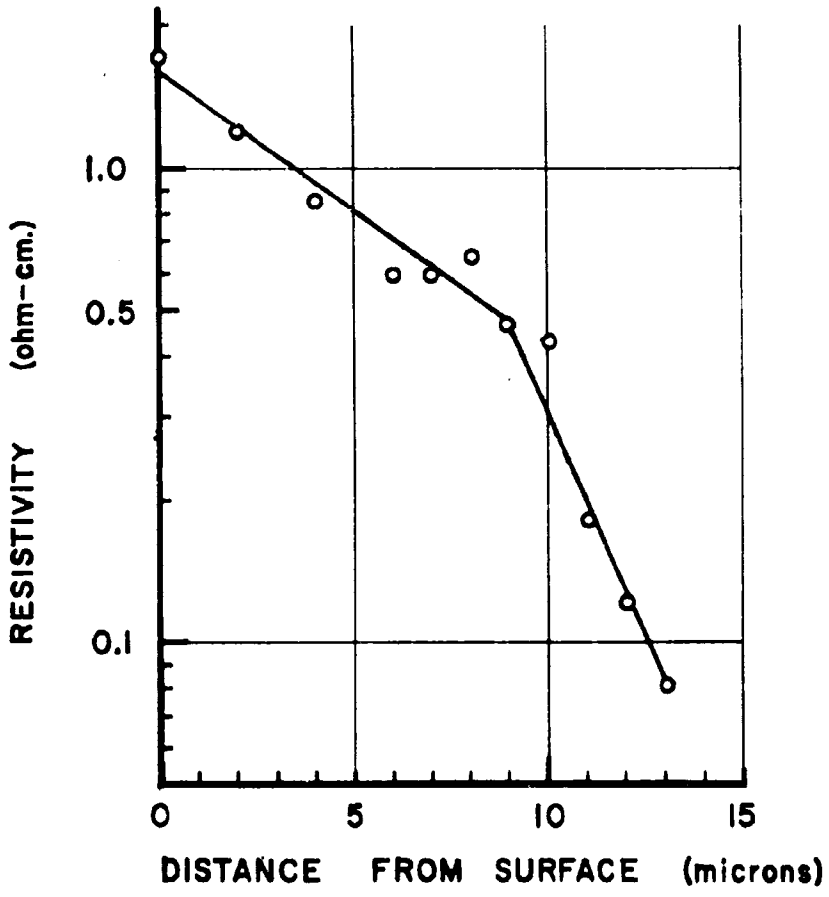


FIGURE II

Metallographic studies indicate that the oxide (when grown at "high" temperatures of approximately 1300°C) has large nucleations that penetrate into the silicon surface below, while oxide layer grown at "low" temperatures (of approximately 1200°C) shows small but very dense numbers of nucleations. In either case, passivated planar diffused diodes made from such material showed low breakdown voltages. Only in regions where no nucleation occurred were the diodes comparable to those that were obtained by conventional passivation processes (i.e., by use of thermally grown oxides).

The work on "in situ" oxidation will be continued in the next quarter. When and if perfected, it will reduce oxidation times by an order of magnitude.

A typical sample of CO_2-$SiCl_4$ grown oxide (over a silicon epitaxial wafer) is shown in FIGURE 12. This oxide film was about 4500 Å thick, grown with the addition of 1 per cent CO_2 at 1250°C (in five minutes). There is a considerable amount of nucleation in polycrystalline silicon dopant over the oxide in the center area of the slice. The edge of the slice was clear and oxide film growth was normal.

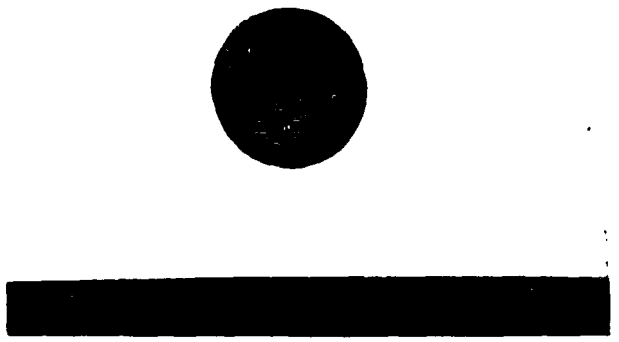
1.6 Oxide-Masked Epitaxial Growth

As reported earlier, oxide masked epitaxial growth (using small etched-out openings in the oxide layer) results in non-uniform epitaxial layers within the openings. These layers tend to have a dish-shaped configuration. Also, as reported previously, the epitaxial growth rate is increased in the presence of an oxide surface. It appears plausible to assume, therefore, that the dish-shaped epitaxial layers are caused by an increasing epitaxial growth rate as one approaches the edge of the oxide window.

If the oxide surface is reduced to the minimal amount, required for the delineation

FIGURE 12

"IN SITU" CO_2-$SiCl_4$ GROWN SILICON OXIDE FILM OVER SILICON EPITAXIAL WAFER



of the growth area only, one might expect that the epitaxial growth rate would more likely be uniform. For this purpose, KPR masking techniques have been used whereby each growth area is delineated by a peripheral oxide border 1 mil wide. Slices grown by the peripheral masking techniques have indeed resulted in the flatter epitaxial layers (see FIGURE 13).

An additional advantage of the peripheral oxide masking technique is due to the elimination or minimization of spurious silicon deposits over the oxide. There is often a spurious overgrowth of polycrystalline silicon on the oxide surface adjoining the windows. This overgrowth is very non-uniform. Oxide areas close to open areas are less affected than the areas further away. The total amount of polycrystalline silicon overgrowth can then be substantially reduced by providing more open areas, as is the case with the peripheral oxide stripe masking technique. The open areas with no oxide protection probably serve as additional nucleation centers for epitaxial growth. This reduces the chance for the supersaturation of silicon compounds or radicals necessary for the nucleation of silicon deposition over oxide surface.

FIGURE 13 shows an N-type layer grown over a P-type substrate with only peripheral oxide masking. The layer is now flat to the edge of the oxide window. There is no nucleation of polycrystalline silicon growth on the oxide stripe.

In FIGURE 14 the bevel-stained crossection of oxide-masked growth of an N-type layer over a P-type substrate is shown. The layer becomes quite non-uniform near the edge of the oxide, and tends to have a dish-shaped configuration. There is also some spurious nucleation of polycrystalline silicon growth over the oxide.

Further work in this area will be directed toward relaxing the 1 mil dimension of the oxide border, since the KPR work at these dimensions is quite tedious and time consuming. If a wider border is feasible, the KPR alignment masking processes will become much simpler.

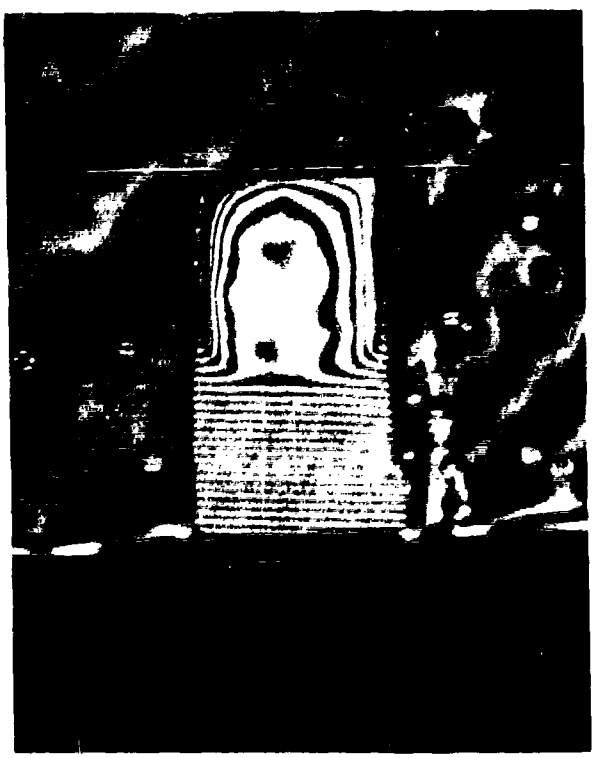
FIGURE 13

MASKED EPITAXIAL GROWTH BY MEANS OF PERIPHERAL OXIDE STRIPE

FIGURE 14

MASKED EPITAXIAL GROWTH BY MEANS OF

CONTINUOUS OXIDE



1.7 Analysis of Doping Gradient Profile in Epitaxial Layers for Integrated Circuit Applications

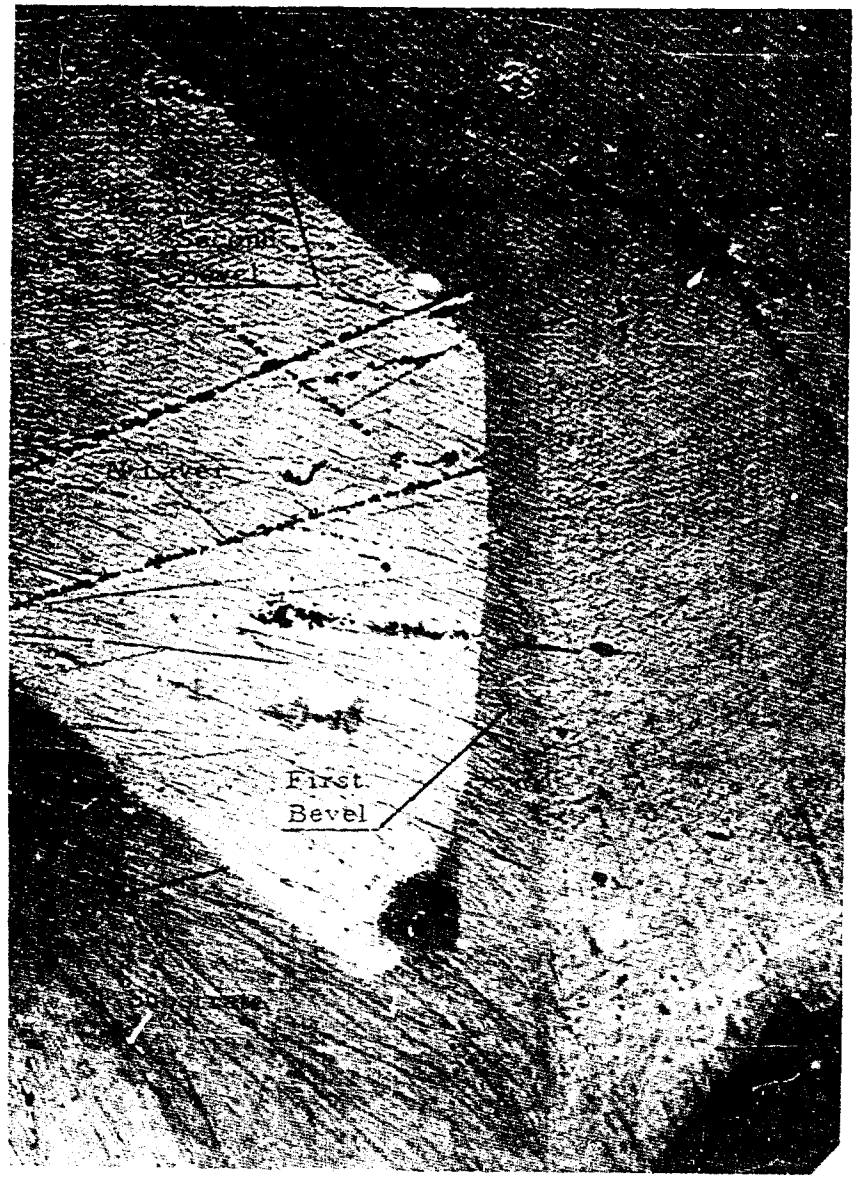
In the Sixth Quarterly Report the two techniques developed for the preparation of epitaxial N/P layers of desirable doping gradient profile for integrated circuit applications were discussed. Intensive study on the sub-epitaxial diffusion approach was carried out during this Quarter. The process consists of pre-diffusing phosphorus or arsenic into selected areas on the 10 ohm-centimeter P-substrate. A thin N-type epitaxial layer is grown over this N-diffused P-type substrate. During the boron diffusion operation, the N+ areas are back-diffusing into the N layer. It is important to know the doping profile in the N+N layer to optimize the circuit performance. The variables here are the surface concentration and nature of the pre-deposited source, the diffusion time and temperature, the N-type layer resistivity, and the growth conditions.

The double bevel diffusion technique developed at Sylvania has been used to analyze the N+N layer (ref. to Second Quarterly Report). Briefly, the epitaxial wafer sample is beveled and subjected to a gallium diffusion treatment. The diffused junction produced in the reference slice is delineated by a standard bevel-staining technique. The diffused junction produced in the beveled surface is delineated by beveling and staining and the depth of penetration measured. The diffused junction depth along the beveled surface gives the profile of the layer resistivity versus layer thickness. These graphical analyses are then correlated with the actual performance of the circuits. The objective here is to reduce the series resistance in Sylvania High Level (SUHL) logic integrated circuits to less than 10 ohms. The desirability of low series resistance was discussed in the Sixth Quarterly Report.

In FIGURE 15, the delineated epitaxial layer structure after gallium diffusion is shown. In this case, an N-type epitaxial layer was grown on a phosphorus pre-diffused P-type substrate of 10 ohm-centimeter resistivity. The stained P-diffused region is constant along the first bevel, and almost equivalent to the depth of the

FIGURE 15

DOPING GRADIENT PROFILE OF N/P EPITAXIAL LAYER WITH PHOSPHORUS PREDIFFUSION



junction along the second bevel. This indicates a rather constant resistivity in the N-layer. The phosphorus prediffusion apparently was not effective in producing the N+ region desired for this structure.

FIGURE 16 is a delineated epitaxial layer structure (after gallium diffusion) with a prediffused arsenic concentration of less than 2×10^{18} atoms/cm^3. Regions with and without arsenic prediffusion are shown. In the area where there is a prediffused arsenic source, there is back-diffusion into the P-substrate. The region with no arsenic prediffusion is clearly seen to the left. There is a graded gallium-diffused P-region along the first bevel, indicating compensation of the arsenic-diffused region by the gallium diffusion. The doping profile can be analyzed according to discussions in the Third Quarterly Report.

FIGURE 17 is a similarly delineated epitaxial structure with a prediffused arsenic concentration of greater than 2×10^{18} atoms/cm^3. Along the first bevel the arsenic back-diffusion shows the embedded N+ region. The graded P-region along the first bevel indicates the high resistivity N-layer doping profile. In this region the transistors and resistors of the integrated circuit will be made.

Integrated circuits fabricated from similar epitaxial layers will be assembled and evaluated. Results will be reported at a later date.

FIGURE 16

DOPING GRADIENT PROFILE OF N/P EPITAXIAL LAYER WITH ARSENIC PREDIFFUSION

(Prediffused Arsenic Concentration)
$< 2 \times 10^{18}$ atoms/cm^3

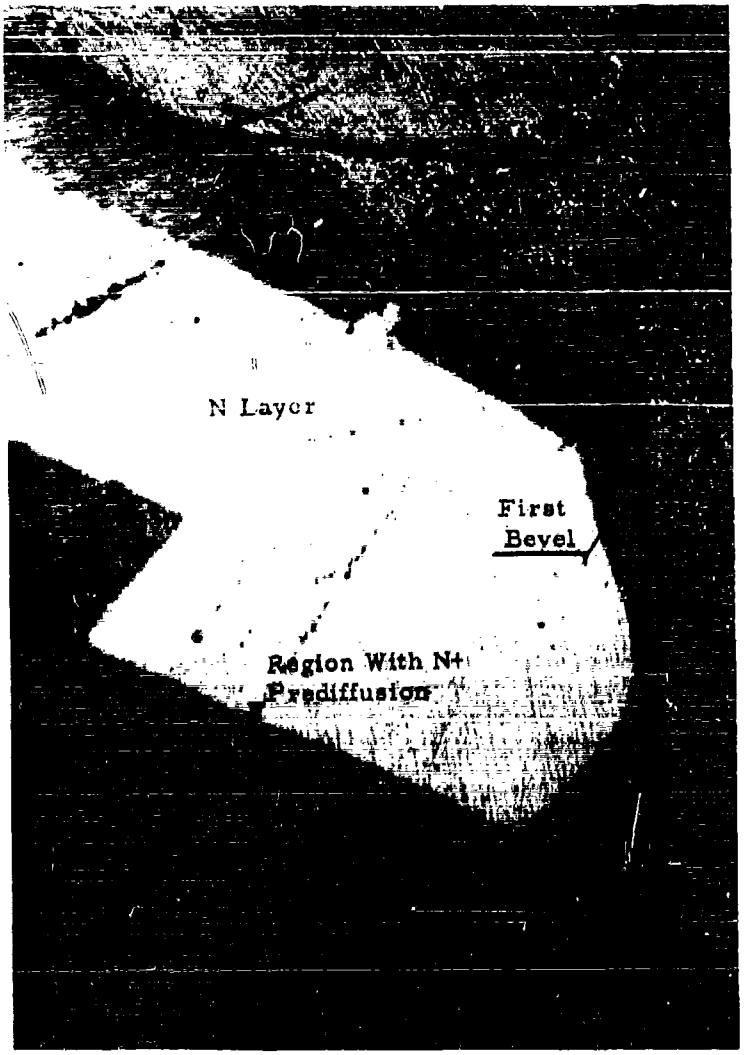


FIGURE 17

DOPING GRADIENT PROFILE OF N/P EPITAXIAL LAYER
WITH ARSENIC PREDIFFUSION

(Prediffused Arsenic Concentration)
$> 2 \times 10^{18}$ atoms/cm^3

1.8 High Voltage, Large Area Epitaxial Planar Junctions As a Means for Evaluation of Epitaxial Layer Quality

Work in this area has been confined to diodes with two types of geometry: one is a circular design (50 mils in diameter) and the other a square design (with sides 100 mils long and rounded corners).

In general, we have used epitaxial layers 2 to 3 1/4 mils thick with resistivities ranging from 20 to 60 ohm-cm. The diffusion depths are 1 to 2 mils, and the C_o of the boron diffusion about 10^{19} atoms/cc.

It has been found that the diode reverse voltages depend largely on the depth of diffusion, or, if reach-through occurs, on the thickness of the epitaxial layer. The resistivity of the layer does not have much effect on the diode reverse voltage, and the only effect due to different geometries is a slightly lower yield and higher leakage currents of the square geometry devices (due to larger areas).

The plans for the next quarter include growing of thicker epitaxial layers (up to 4 mils), and diffusions to a depth of 2 to 3 mils. This is expected to give reverse voltages in the range of 500 to 700 volts, compared with the present 400 to 500 volts. (Note: Leakage currents were in the order of tenths of a μA at 300 volts). Due to the present type of mounting, the forward characteristics have been rather poor (about 1 amp at 1 volt), but it is hoped that with the new mounting techniques this parameter can be improved considerably.

2.0 Study of Vapor Growth of Silicon Thin Films on Foreign Substrates

During the course of the work on this project, it became evident that there were a number of distinct, albeit interdependent, factors required for the successful production of device-quality silicon films on unconventional substrates. These are listed and briefly discussed below in order of their occurrence during the process:

2.1 Substrate:

a) Surface smoothness:

This has been a serious problem, somewhat overcome by the multiple glass deposition/firing cycles as discussed in the last quarterly report. New ceramic substrates have been obtained with approximately a micron roughness -- at least an order of magnitude improvement in surface smoothness. Silicon deposited directly on this substrate is among the best looking deposit prepared to date.

b) Thermal expansion coefficient:

There is need for a matching of thermal expansion coefficients between the depositing crystalline silicon film, the ceramic substrate, and the glass interlayer. Silicon has an expansion coefficient of $4.2 \times 10^{-6}/^{\circ}C$, alumina has a value between 6 and $9 \times 10^{-6}/^{\circ}C$ (depending on purity), while the glasses that have been used have values in the 10^{-6} range. Some of the glasses used will support silicon films without the silicon "popping off", whereas, other glasses used will not (see discussion in 2.2 below).

c) Single crystal:

Since it would be desirable to use single crystal films for device fabrication, a compatible insulating single crystal substrate clearly would be

expected to be a successful substrate. Two such materials have been briefly evaluated: beryllium oxide (expansion coefficient 5.8 x $10^{-6}/^{\circ}C$) and single crystal sapphire (approximately 8 x $10^{-6}/^{\circ}C$). No conclusive proof has been obtained (by Laue X-ray photography or by electron microscopy) that the silicon films on the single crystal ceramic substrates were themselves single crystal. However, the enclosed photograph (FIGURE 18) of a very thin silicon deposit on single crystal beryllia shows preferred orientation. This is shown by series of parallel growth lines at each end of the photograph and at an angle to each other. Shown in FIGURE 19 is a deposit of silicon on single crystal sapphire. This example is among the best to date, and is notably improved over the deposits reported in the previous Quarterly Report.

2.2 Glass:

Some important interrelated parameters of the glass are:

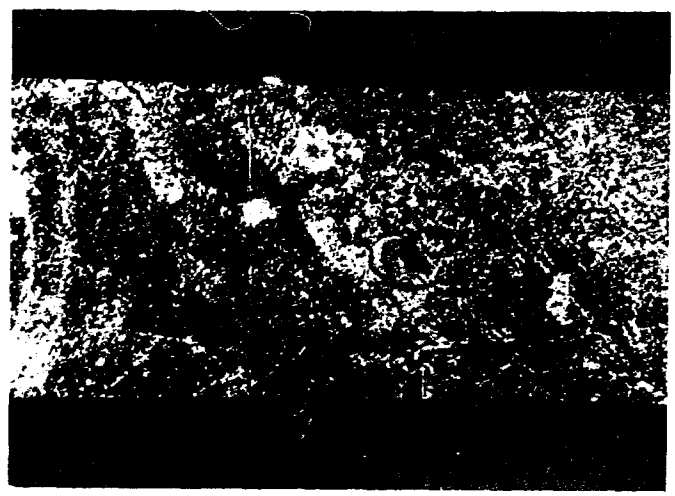
a) composition,
b) thermal expansion coefficient,
c) softening temperature,
d) viscosity, and
e) chemical inertness.

We have tried a series of glasses with thermal expansion coefficients ranging from 5 to 9 x $10^{-6}/^{\circ}C$. The deposited silicon adheres quite well to some of these glasses, whereas with others, the silicon pops off the glass easily. The observations and data are being rechecked for accuracy and will be reported in more detail in the next Quarterly Report.

Another glass parameter of technological importance is the particle size. The glass is currently being ground to the order of a micron in size, rather than to the earlier (10 or more microns) size particles. Smaller particle sizes appear to give improved glass film smoothness.

FIGURE 18

VAPOR DEPOSITED SILICON THIN FILM OVER
SINGLE CRYSTAL BERYLLIUM OXIDE



MAGNIFIED
60 TIMES

FIGURE 19

VAPOR DEPOSITED SILICON THIN FILM OVER
SINGLE CRYSTAL SAPPHIRE

MAGNIFIED
75 TIMES

2.3 Glass Film Deposition Technique

Variables in this area include:

a) substrate preparation - especially substrate cleanliness,
b) thickness of glass deposited - currently running in the order of a micron,
c) glass settling techniques - specifically, evaluation of a centrifuge technique, as well as a gravity settling method,
d) glass firing and cooling procedures.

One of the recurring problems is a pronounced non-uniformity of deposited glass, both before and after firing. Various bubbles and irregularities in the deposited glass were noted, which plague efforts to produce good quality silicon deposits over such glass films. This is an area in which much progress can and must be made. The influence of these factors on initiating devitrification is another area that requires investigation.

2.4 Silicon Film Growth Technique

Important variables here include:

a) growth temperature,
b) gas flow rate and flow pattern,
c) preanneal time,
d) preheating and/or supercolling effects,
e) nucleation,
f) final growth rate,
g) thickness of film growth, and
h) cooling rate.

Because some of the worked-on glasses had such low viscosity that the glass largely flowed off the ceramic wafer at the elevated growth temperature (1175°C), an attempt was made to determine the lowest practical growth temperature for this system. The lowest temperature to achieve single crystal silicon epitaxial film growth over single crystal silicon substrate was found to be at about 975°C. This was then taken to be the lowest practical temperature for thin film growth in the present system. A somewhat higher temperature will then be used to try to grow silicon onto the low viscosity glass.

2.5 Evaluation of Growth

Parameters being examined her include:

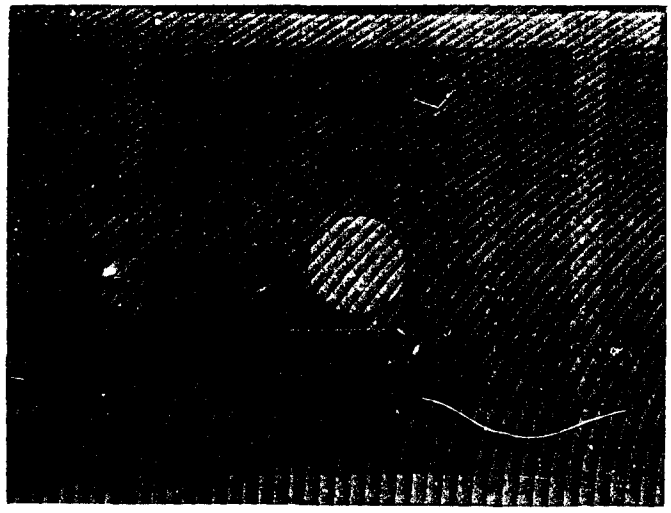
a) stresses in the films producing curvature and "popping off" of silicon,
b) optical appearance, such as roughness, metallic luster, etc., and
c) the degree of crystalline perfection to determine oriented grain growth, grain size, etc.

2.6 Oxide Window Preparation

Pyrolytically produced silicon dioxide films have been deposited on silicon films that were in turn deposited on ceramic substrate, and also on glass over ceramic substrate. By means of standard planar KPR techniques, windows in the oxide are opened, as shown in FIGURE 20. PN junctions will be prepared for evaluation of the quality of the deposited silicon film. We find that the quality of the windows, such as sharpness of definition, etc., is a function of the surface roughness of the film. This is an area that is currently being investigated.

FIGURE 20

PYROLYTIC OXIDE WINDOW OVER SILICON THIN FILM
DEPOSITED OVER ALUMINA CERAMIC SUBSTRATE



MAGNIFIED
150 TIMES

2.7 Epitaxial Growth of P Layers Within Oxide Windows

A second epitaxial growth furnace is being modified with parts just received, in order to grow epitaxial P layers within the oxide windows. Following this, the resulting device parameters will be determined and used as an indicator of the quality of the silicon film produced.

3.0 Conclusions

3.1 A control of layer thickness and resistivity of ±5 per cent within a run and less than ± 10 per cent from run to run has been achieved for the N/P epitaxial layers for the fabrication of high level logic silicon integrated circuits. This is believed to be the limit of accuracy of measurement techniques and the limit of the present epitaxial growth furnace capability.

3.2 With HCl vapor phase etching and palladium diffusion-purified hydrogen in the growth cycle, the epitaxial layers grown show practically no stacking faults except at the edge. The dislocation density of the layer is about the same as that of the substrate.

3.3 The measurement of junction capacitance on step-etched layer specimens appears as a useful tool for the analysis of doping gradient profile in P/P+ epitaxial layers.

3.4 It appears likely that a prior hydrogen fluoride cleaning treatment is needed in order to obtain reproducible three point probe breakdown readings in P-type layers.

3.5 CO_2-$SiCl_4$ "in situ" oxidation of silicon epitaxial layers immediately after deposition has not been successful in providing uniform, good quality oxide film such as that obtained by thermal oxidation.

3.6 Peripheral oxide masking is found to yield flat epitaxial deposits in windows with greatly reduced spurious nucleation of polycrystalline silicon growth over oxide.

3.7 The double bevel diffusion technique has been found a very useful tool for the analysis of the doping profile of the N/P epitaxial layer grown on a selectively prediffused substrate.

3.8 From doping profile analysis, selective arsenic prediffusion appears as a promising approach for performance improvement of high level logic integrated circuits.

3.9 Vapor-deposited silicon thin film over single crystal beryllium oxide substrates shows some evidence of growth in the preferred orientation.

3.10 The present growth conditions for the silicon film/glass/ceramic are not ideal for the deposition of high quality silicon film. Much more work must be carried out in this area to perfect this process.

4.0 Program For Next Quarter

Work is planned for the next quarter in the following areas:

4.1 Continue the study of compatible oxide masking techniques for epitaxial growth of improved quality in selected areas.

4.2 Continue to perfect the sub-epitaxial diffusion technique for the preparation of selective NN+ regions in N/P epitaxial layers for integrated digital circuit applications.

4.3 Study the technique for the preparation of epitaxial layers for integrated linear circuit applications.

4.4 Carry out doping profile analysis of epitaxial layers for integrated circuit applications.

4.5 Analyze the doping profiles of abrupt and graded P/P+ epitaxial layers by the step-etching capacitance measurement or other suitable techniques.

4.6 Study the feasibility of capacitance measurement for checking the lateral resistivity variations in the epitaxial N/P layers.

4.7 Continue to explore ways to improve epitaxial layer and surface perfection and to study the layer structure by non-destructive in-process measurement techniques.

4.8 Continue to evaluate the $SiCl_4$-CO_2 process to grow oxide "in situ" over silicon epitaxial layers for surface passivation application.

4.9 Carry out experimental work to establish technology for the preparation of large area, high voltage ($\geq$ 500 volts) epitaxial diffused junctions.

4.10 Continue to explore ways to deposit silicon thin films of improved perfection over non-silicon, dielectric substrates.

4.11 Evaluate silicon thin film deposits over non-silicon, dielectric substrates, both by physical studies and by PN junction formation.

5.0 Identification of Technical Personnel

		21 Month Total Hours (12 mos. Orig. Contract) 9 mos. ext. Mod. 2)
Engineers		
V. Sils		1934.0
A. Coates		1822.5
N. Cerniglia		936.0
J. Porter		11.0
B. Selikson		652.0
H. Posen		305.4
R. Yee		396.0
J. Coulthard		114.0
R. Berkstresser		2524.0
I. Feinberg		134.0
J. Ketseas		159.0
E. Lewis		116.0
J. McManus		212.0
J. Grace		58.0
M. Kahane		264.0
R. Shamash		78.0
J. Sciola		14.0
S. Millman		1205.0
S. Crytzer		62.0
M. Miller		4.0
	Subtotal	11000.9
Technicians		
H. Glidden		1344.0
E. Juleff		535.0
M. Coppinger		6.0
R. Gallo		60.0
A. Hathaway		498.5
B. Davidson		1091.0
R. Waters		85.5
P. Keating		294.0
O. DeSilvestre		1650.0
E. McKenna		2.0
R. Greene		47.0
G. Mann		73.0
M. DeAngeles		68.0
E. Andrews		495.0
P. Rolls		78.0
D. Crawford		20.0
B. Zaffina		28.0
R. Gorman		4.0
M. Jones		24.0
	Subtotal	6408.0

Operators

G. Brown		3.0
D. Doyle		78.0
E. Abele		1327.5
G. Brown		200.5
H. Doucette		34.5
S. Belanger		3.5
K. Hicks		5.0
J. Grande		6.0
E. Kay		408.0
A. Noonan		48.0
	Subtotal	2114.0
	GRAND TOTAL	19,522.9

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